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Specifications

(54) [Title of the Invention] Silicon Wafer, Manufacturing Method Thereof, and Quality Evaluation Method

(57) [Summary]

[Object] The objects of the present invention are to provide at high yield a silicon wafer that is good for production of ultra highly integrated circuitry.

[Composition of the Invention] A silicon single crystal is pulled by the CZ method, followed by slicing, lapping, etching, and mirror polishing. By control of the rate of cooling of the silicon single crystal after solidification, the size distribution of etch pits upon the surface after ammonia-type cleaning is such that the following criterion is satisfied: (total count of 0.13 μm pits and larger) / (total count of 0.11 μm pits and larger) > 0.3.

[Scope of the Patent Claims}

[Claim 1] A silicon single crystal pulled by the CZ method; wherein the silicon wafer produced by slicing, lapping, etching, and mirror polishing of this single crystal has a size distribution of etch pits upon the surface after ammonia-type cleaning such that the following criterion is satisfied: (total count of 0.13 μm pits and larger) / (total count of 0.11 μm pits and larger) > 0.3.

[Claim 2] A silicon single crystal pulled by the CZ method; wherein the silicon wafer produced by slicing, lapping, etching, and mirror polishing of this single crystal has a size distribution of etch pits upon the surface after ammonia-type cleaning such that the following criterion is satisfied: (total count of 0.13 μm pits and larger) / (total count of 0.10 μm pits and larger) > 0.2.

[Claim 3] A method for production of the silicon single crystal of Claim 1 or Claim 2 by pulling silicon single crystal by the Czochralski method; wherein cooling rate during the 1200°C to 950°C post-solidification single crystal cooling step is 2.0°C/minute or less; and the minimum value of cooling rate between 1200°C and 950°C is 1.0°C/minute or less.

[Claim 4] A method for production of the silicon single crystal of Claim 1 or Claim 2 by pulling silicon single crystal by the Czochralski method; wherein cooling rate during the 1200°C to 950°C post-solidification single crystal cooling step is 2.0°C/minute or less; and the minimum value of cooling rate between 1200°C and 950°C is less than or equal to 1.0°C/minute and more than or equal to 0.4°C/minute.

[Claim 5] A method for production of the silicon single crystal of Claim 1 or Claim 2 by pulling silicon single crystal by the Czochralski method; wherein cooling rate during the 1200°C to 950°C post-solidification single crystal cooling step is 2.0°C/minute or less; the minimum value of cooling rate between 1200°C and 950°C is less than or equal to 1.0°C/minute and more than or equal to 0.4°C/minute; and the cooling rate from 950°C to 800°C is 0.6°C/minute or greater.

[Claim 6] A silicon wafer quality evaluation method during which single crystal is pulled by the CZ method, and a silicon wafer is produced by slicing, lapping, etching, and mirror polishing of this single crystal, followed by ammonia type cleaning and measurement of the size and count of etch pits appearing on the surface; wherein crystal defect quality and electrical characteristics within the silicon wafer are evaluated by calculation of the ratio of (total count of 0.13 μm pits and larger) / (total count of 0.11 μm pits and larger) or (total count of 0.13 μm pits and larger) / (total count of 0.10 μm pits and larger).

[Detailed Explanation of the Invention]

[0001]

[Field of Industrial Use]

The present invention relates to a silicon wafer used for the production of semiconductor integrated circuits and more specifically relates to a silicon wafer used for integrated circuits of at least 1 M capacity.

[0002]

[Conventional Technology]

Generally a silicon wafer used for semiconductor integrated circuits is produced by pulling silicon single crystal by the Czochralski method (referred to hereinafter as the CZ method), followed by slicing, lapping, etching, polishing, and a final wash step to remove surface contamination and particles.

[0003] However, numerous minute etch pits are known to exist upon the surface of this silicon wafer as mentioned, for example, in Published Unexamined Patent Application No. Hei 3-275598. This publication indicates that the defects, known as OSFs (oxidation induced stacking faults), forming these etch pits are heterogeneous. Moreover, this publication mentions that such etch pits can be counted using a particle counter, that a wafer that has pits of at least 0.2 μm can be used for 4 MB and greater capacity DRAM, and that cooling rate of the crystal during the stage from melt-freezing to 900°C should be at least 1.2°C/minute in order to decrease those pits that are 0.2 μm and larger.

[0004] Moreover, similar conventional technology is mentioned in Published Unexamined Patent Application No. Hei 4-42893. This publication discloses that these etch pits harm electrical characteristics of the wafer and proposes during cooling of the pulled silicon single crystal that cooling rate should be decreased to 0.4°C/minute or less during the 1200°C to 800°C temperature interval in order to eliminate 0.2 μm etch pits.

[0005]

[Problems to be Solved by the Invention] However, it has become clear now as the degree of integration of integrated circuits increases that simple elimination of 0.2 μm and larger pits won't provide a sufficient device yield. For example, just using a wafer having no 0.2 μm or larger pits as a silicon

wafer for 16 MB DRAM doesn't provide a sufficiently high yield. Even when a wafer is used for 4 MB DRAM or 1 MB DRAM that has no 0.2 μm or larger pits, due to appropriateness or inappropriateness of the match between the wafer and device processes, it is clear that a good yield isn't always provided. Therefore a need exists for a silicon wafer that has good electrical characteristics and that provides high device yield.

[0006] Furthermore, as the degree of integration increases from 64 M to 256 M, the above mentioned conventional technology is anticipated to not provide a sufficiently high device yield. Therefore a silicon wafer is needed that has even better electrical characteristics.

[0007] Therefore the object of the present invention is to provide a high quality silicon wafer that has excellent electrical characteristics and that provides a high device yield even when used for integrated circuits that have a high degree of integration.

[0008]

[Means to Solve the Problems] The present invention is a silicon single crystal pulled by the CZ method; wherein the silicon wafer produced by slicing, lapping, etching, and mirror polishing of this single crystal has a size distribution of etch pits upon the surface after ammonia-type cleaning such that the criterion of (total count of 0.13 μm pits and larger) / (total count of 0.11 μm pits and larger) > 0.3 or (total count of 0.13 μm pits and larger) / (total count of 0.10 μm pits and larger) > 0.2 is satisfied, thereby providing a high quality silicon wafer that has excellent electrical characteristics.

[0009]

[Operation of the Invention] The inventors of the present invention, as a result of accumulated and quite careful research relating to the relationship between ammonia-type-washing-induced etch pits and device yield, discovered that variance in device yield for high integration circuits wasn't just due to crystalline defects that form 0.2 μm etch pits and larger. Rather, crystalline defects that form even smaller etch pits were found to affect device yield. The relationship between crystalline defects that form etch pits and pn junction leakage and gate oxide layer insulation breakdown voltage, which are important for device yield, will be explained in detail below.

[0010] The gate oxide layer is formed from SiO_2 by oxidation of Si of the silicon wafer in an oxygen atmosphere at roughly 1000°C. When crystalline defects are present within the silicon wafer, such defects are known to also exist within the gate oxide layer as weak spots that degrade the insulation breakdown voltage. However, gate oxide layer thickness of devices formed upon silicon wafers has become thin in accompaniment with increased integration of recent devices. Although the conventional thickness has been 25 to 15 nm, this has become 10 nm to several nm for recent 4 M and 16 M DRAM. In accompaniment with this trend, crystalline defects that degrade breakdown voltage of the gate oxide layer have come to be seen as a problem at a smaller size than before. Specifically, although crystalline defects as large as 12 nm are permissible when gate oxide layer thickness is 20 nm, 5 nm

crystalline defects aren't permissible when gate oxide layer thickness becomes 10 nm (e.g., see K. Yamabe, Y. Ozawa, S. Nadahara, and K. Imai, "Thermally Grown Silicon Dioxide with High Reliability," Semiconductor Silicon, pp. 346 - 363 (1990)). If defects larger than this are present within the oxide film, failures occur such as switching operation failures, etc. such that device yield decreases.

[0011] Next, pn junction leakage will be discussed. As the degree of integration of devices increases, the absolute value of capacitance decreases as capacitor surface area per bit unit of memory decreases. Also since the time interval of the refresh operation (time required to inject a charge in order to continue retention of memory) must be prolonged in response to the need for lower power consumption, the resultant leakage current must be prevented. However, when metal contamination or crystalline defects form a deep energy level (an energy level positioned in the vicinity of the bandgap center of growth-recombination of electrons-holes within the hole layer of this pn junction interface), charge leaks occur to form a leakage current. Although increased cleanliness has been previously used to prevent metal contamination, crystalline defects in the silicon wafer will need to be earnestly reduced in the future in order to reduce the origins of leakage.

[0012] In consideration of the above mentioned two standpoints, silicon single crystal was pulled under various conditions, and etch pits equal to or less than 0.2 μm were examined. It was therefore found that conditions of single crystal pulling could affect the size distribution in various ways. Furthermore, when wafers produced from such silicon single crystal were used, and when the relationship with device yield was examined, it was found that the adverse effect upon device yield was small for defects that grow into relatively large pits, and it was found that the adverse effect upon device yield was large for defects that form relatively small sized pits.

[0013] Characteristics and the formation method of the defects that form etch pits, as well as the effect of such defects upon device yield, can be explained as follows. That is to say, interstitial silicon and voids introduced at the melt-solid interface become supersaturated during the subsequent cooling step. These mutually react, accumulate, and combine, and also combine with oxygen which has also become similarly supersaturated. Such defects are selectively etched by ammonia-type washing to form etch pits. However, the size of such etch pits is determined by the size and morphology of these defects. According to experiments of the inventors of the present invention, defects that cause the formation of relatively large size etch pits (i.e., defects that cause the formation of etch pits equal to 0.13 μm and larger) are characterized in that such defects readily dissolve and disappear due to heat treatment. Since during the oxide layer formation step occurring at 900°C to 1000°C during device processing, or during the well diffusion step at 1100°C to 1250°C, shrinkage and disappearance is relatively easy, interference occurs within the oxide layer, and a defect-induced deep energy level doesn't remain at the pn junction interface of the hole layer. Therefore even if such defects are present in the silicon wafer or silicon single crystal prior to device processing, such defects disappear during device processing so that such defects don't have an adverse effect, which results in a high device yield.

[0014] On the other hand, the defects which cause the formation of comparatively small size etch pits (i.e., defects which cause formation of etch pits that are 0.13 μm and smaller) are stable with respect to heat treatment. Such defects disappear with difficulty during the oxide layer formation step occurring at 900°C to 1000°C during device processing or during the well diffusion step at 1100°C to 1250°C. Therefore interference occurs within the oxide layer, and a defect-induced deep energy level remains at the pn junction interface of the hole layer. Therefore when devices are formed upon a silicon wafer as a substrate that contains numerous such defects, problems arise such as the occurrences of oxide layer breakdown voltage insulation failure and high refresh failure rate due to high leakage current so that device yield drops.

[0015] However, the inventors of the present invention discovered that control of the rate of cooling of the post-solidification single crystal within a certain range made possible control of the size of such defects. For example, when the cooling rate from 1200°C to 950°C is decreased during the post-solidification single crystal cooling step, crystal defects that form 0.13 μm and larger etch pits increase. When the cooling rate from 950°C to 800°C increases, the crystal defects that form 0.13 μm and smaller etch pits increase.

[0016] Good cooling rate ranges for obtaining the etch pit size distribution of the present invention are the following: a cooling rate less than or equal to 2.0°C/minute between 1200°C to 950°C during the post-solidification single crystal cooling step, a minimum value of cooling rate less than or equal to 1.0°C/minute between 1200°C to 950°C; and more preferably, a cooling rate less than or equal to 2.0°C/minute between 1200°C to 950°C during the post-solidification single crystal cooling step, and a minimum value of cooling rate less than or equal to 1.0°C/minute and greater than or equal to 0.4°C/minute between 1200°C to 950°C. A lowest cooling rate of at least 0.4°C/minute is specified since a lower cooling rate than that value isn't particularly effective and since an extreme lowering of cooling temperature would result in a lowering of pull rate and productivity. [*TRANSLATOR'S NOTE: This looks like an error in the source text. Probably this was supposed to say "an extreme lowering of cooling rate."*]

[0017] Moreover, a more preferred cooling rate range is the following: a cooling rate less than or equal to 2.0°C/minute between 1200°C to 950°C during the post-solidification single crystal cooling step, a minimum value of cooling rate less than or equal to 1.0°C/minute and greater than or equal to 0.4°C/minute between 1200°C to 950°C, and a cooling rate greater than or equal to 0.6°C/minute between 950°C to 800°C. The cooling rate over the interval of 950°C to 800°C is specified for reasons such as those explained above in order not to cause an increase in crystalline defects which form 0.13 μm and smaller etch pits.

[0018] Furthermore, lower limit of etch pit size is set to 0.10 μm or 0.11 μm since the utilized particle counter then has good resolution performance, and more fundamentally, since defects that cause the formation of etch pits larger than 0.13 μm have little adverse effect upon device yield, and since defects

that cause the formation of smaller etch pits are thought to have a major adverse effect upon device yield.

[0019]
[Working Examples] Working examples of the present invention are explained below.
<Working Example 1> Figure 1 shows a CZ method type pulling apparatus for use for the present invention. Within this figure, a freely rotatable graphite crucible 3 was disposed within a chamber 2 equipped with a gas discharge port 1 and a (non-illustrated) gas feed port. A silica glass crucible 4 was inserted into this crucible 3. The size of graphite crucible 3 and silica glass crucible 4 was 16 inches. A (non-illustrated) pull cable was placed above these crucibles and held a seed crystal by means of a chuck 5 at the tip of the pull cable. Moreover, a heater 6 and carbon fiber molded insulation member 7 were placed at the perimeter of the crucibles. Furthermore, in order to restrict cooling rate of the post-solidification silicon single crystal to a certain range, a downwardly expanding thermal reflector 9 was placed so as to surround silicon single crystal 8 within the furnace. Thermal reflector 9 was formed from carbon fiber molded thermal insulation material. After a 45 kg charge of polysilicon loaded into this silica glass crucible 4 was melted, a 6 inch size silicon single crystal was pulled at a pull rate of 1.0 to 1.2 mm/minute. Cooling rate was controlled in the range indicated by Table 1.

[0020] This silicon single crystal was processed by the normal processing method comprising slicing, edge rounding, lapping, etching, and polishing. Thereafter ammonia-type washing (NH_4OH : H_2O_2 : H_2O = 1 : 1 : 5) was carried out. Temperature of the washing solution was 80°C, and 2 washes (10 minutes each) were performed for a total of 20 minutes of washing time. Etch pits generated upon this wafer were then measured using a laser-type particle counter (LS600, manufactured by Hitachi Electronics Engineering Corp.). These results are shown in Table 1 and Table 2.

[0021] Moreover, an oxide layer about 25 nm thick was formed upon this 6 inch size silicon wafer. Then 200 two-layer gate electrodes of 5 mm diameter were formed upon this oxide layer comprising an upper layer of aluminum and a lower doped layer. Into each of these respective MOS diodes were injected numerous carriers from the substrate silicon as DC polarized voltage was applied between the electrodes at the aluminum layer and the substrate silicon backside. This voltage was ramped upward step-wise in electric field increments equivalent to 0.25 MV/cm each. Holding period for each step was 200 msec as leakage current was measured as the voltage gradually increased. The value of applied voltage when leakage current reached 1 $\mu A/cm^2$ was placed into one of three categories as shown in Table 2: less than 6 MV/cm, between 6 and 8 MV/cm, and greater than 8 MV/cm.

[0022] Moreover, a six inch size mirror polished silicon wafer was produced from the same silicon single crystal in the same manner. Then 200 dynamic-type RAM were formed upon this wafer using 1.3 μm design rule. Bit failure was measured at a refresh time period (time period between a given injection of charge and the following injection of charge) of 512 cycles per 8 msec. The resultant refresh failure rate is shown in Table 2.

[0023] <Working Example 2> Figure 2 shows a CZ method type pulling apparatus for use for the present invention. Within this figure, a freely rotatable graphite crucible 3 was disposed within a chamber 2 equipped with a gas discharge port 1 and a (non-illustrated) gas feed port. A silica glass crucible 4 was inserted into this crucible 3. The size of graphite crucible 3 and silica glass crucible 4 was 18 inches. A (non-illustrated) pull cable was placed above these crucibles and held a seed crystal by means of a chuck 5 at the tip of the pull cable. Moreover, a heater 6 and carbon fiber molded insulation member 7 were placed at the perimeter of the crucibles. Furthermore, in order to restrict cooling rate of the post-solidification silicon single crystal to a certain range, a 300 mm inside diameter and 100 mm tall crystal heater 10 was mounted within the furnace so as to surround silicon single crystal 8. During the entire time period between pulling of the crown region until formation of the tail region, 7 kW was applied to this heater. After a 55 kg charge of polysilicon loaded into this silica glass crucible 4 was melted, an 8 inch size silicon single crystal was pulled at a pull rate of 0.8 to 1.0 mm/minute. Cooling rate was controlled in the range indicated by Table 1.

[0024] This silicon single crystal was processed by the normal processing method comprising slicing, edge rounding, lapping, etching, and polishing. Thereafter ammonia-type washing ($NH_4OH : H_2O_2 : H_2O = 0.2 : 1 : 10$) was carried out. Temperature of the washing solution was 80°C, and 2 washes (10 minutes each) were performed for a total of 20 minutes of washing time. Etch pits generated upon this wafer were then measured using a laser-type particle counter (LS600, manufactured by Hitachi Electronics Engineering Corp.). These results are shown in Table 1 and Table 2.

[0025] Moreover, an oxide layer about 25 nm thick was formed upon this 8 inch size silicon wafer. Then 368 two-layer gate electrodes of 5 mm diameter were formed upon this oxide layer comprising an upper layer of aluminum and a lower doped layer. Into each of these respective MOS diodes were injected numerous carriers from the substrate silicon as DC polarized voltage was applied between the electrodes at the aluminum layer and the substrate silicon backside. This voltage was ramped upward step-wise in electric field increments equivalent to 0.25 MV/cm each. Holding period for each step was 200 msec as leakage current was measured as the voltage gradually increased. The value of applied voltage when leakage current reached 1 $\mu A/cm^2$ was placed into one of three categories as shown in Table 2: less than 6 MV/cm, between 6 and 8 MV/cm, and greater than 8 MV/cm.

[0026] Moreover, an eight inch size mirror polished silicon wafer was produced from the same silicon single crystal in the same manner. Then 368 dynamic-type RAM were formed upon this wafer using 1.3 μm design rule. Bit failure was measured at a refresh time period (time period between a given injection of charge and the following injection of charge) of 512 cycles per 8 msec. The resultant refresh failure rate is shown in Table 2.

[0027] <Working Example 3> Figure 3 shows a CZ method type pulling apparatus for use for the present invention. Within this figure, a freely rotatable graphite crucible 3 was disposed within a

chamber 2 equipped with a gas discharge port 1 and a (non-illustrated) gas feed port. A silica glass crucible 4 was inserted into this crucible 3. The size of graphite crucible 3 and silica glass crucible 4 was 18 inches. A (non-illustrated) pull cable was placed above these crucibles and held a seed crystal by means of a chuck 5 at the tip of the pull cable. Moreover, a heater 6 and carbon fiber molded insulation member 7 were placed at the perimeter of the crucibles. Furthermore, in order to restrict cooling rate of the post-solidification silicon single crystal to a certain range, a 260 mm inside diameter and 100 mm tall crystal heater 10 was mounted within the furnace so as to surround silicon single crystal 8. During the entire time period between pulling of the crown region until formation of the tail region, 15 kW was applied to this heater. In order to cause cooling of the crystal immediately above crystal heater 10, the head was squared off rather than given a dome shape. After a 50 kg charge of polysilicon loaded into this silica glass crucible 4 was melted, a 6 inch size silicon single crystal was pulled at a pull rate of 0.9 to 1.1 mm/minute. Cooling rate was controlled in the range indicated by Table 1.

[0028] This silicon single crystal was processed by the normal processing method comprising slicing, edge rounding, lapping, etching, and polishing. Thereafter ammonia-type washing (NH_4OH : H_2O_2 : H_2O = 3 : 1 : 5) was carried out. Temperature of the washing solution was 80°C, and 2 washes (10 minutes each) were performed for a total of 20 minutes of washing time. Etch pits generated upon this wafer were then measured using a laser-type particle counter (LS600, manufactured by Hitachi Electronics Engineering Corp.). These results are shown in Table 1 and Table 2.

[0029] Moreover, an oxide layer about 25 nm thick was formed upon this 6 inch size silicon wafer. Then 200 two-layer gate electrodes of 5 mm diameter were formed upon this oxide layer comprising an upper layer of aluminum and a lower doped layer. Into each of these respective MOS diodes were injected numerous carriers from the substrate silicon as DC polarized voltage was applied between the electrodes at the aluminum layer and the substrate silicon backside. This voltage was ramped upward step-wise in electric field increments equivalent to 0.25 MV/cm each. Holding period for each step was 200 msec as leakage current was measured as the voltage gradually increased. The value of applied voltage when leakage current reached 1 $\mu A/cm^2$ was placed into one of three categories as shown in Table 2: less than 6 MV/cm, between 6 and 8 MV/cm, and greater than 8 MV/cm.

[0030] Moreover, a six inch size mirror polished silicon wafer was produced from the same silicon single crystal in the same manner. Then 200 dynamic-type RAM were formed upon this wafer using 1.3 μm design rule. Bit failure was measured at a refresh time period (time period between a given injection of charge and the following injection of charge) of 512 cycles per 8 msec. The resultant refresh failure rate is shown in Table 2.

[0031] <Working Example 4> Figure 4 shows a CZ method type pulling apparatus for use for the present invention. Within this figure, a freely rotatable graphite crucible 3 was disposed within a chamber 2 equipped with a gas discharge port 1 and a (non-illustrated) gas feed port. A silica glass crucible 4 was inserted into this crucible 3. The size of graphite crucible 3 and silica glass crucible 4 was

22 inches. A (non-illustrated) pull cable was placed above these crucibles and held a seed crystal by means of a chuck 5 at the tip of the pull cable. Moreover, a heater 6 and carbon fiber molded insulation member 7 were placed at the perimeter of the crucibles. Furthermore, in order to restrict cooling rate of the post-solidification silicon single crystal to a certain range, a 280 mm inside diameter and 70 mm tall crystal heater 10 was mounted within the furnace so as to surround silicon single crystal 8. During the entire time period between pulling of the crown region until formation of the tail region, 15 kW was applied to this heater. Also a thermal insulator 12 was placed surrounding the heater so that heat from the heater would reach silicon crystal 8 with good efficiency. After a 100 kg charge of polysilicon loaded into this silica glass crucible 4 was melted, an 8 inch size silicon single crystal was pulled at a pull rate of 0.7 to 0.9 mm/minute. Cooling rate was controlled in the range indicated by Table 1.

[0032] This silicon single crystal was processed by the normal processing method comprising slicing, edge rounding, lapping, etching, and polishing. Thereafter ammonia-type washing (NH_4OH : H_2O_2 : H_2O = 1 : 1 : 5) was carried out. Temperature of the washing solution was 80°C, and 2 washes (10 minutes each) were performed for a total of 20 minutes of washing time. Etch pits generated upon this wafer were then measured using a laser-type particle counter (LS600, manufactured by Hitachi Electronics Engineering Corp.). These results are shown in Table 1 and Table 2.

[0033] Moreover, an oxide layer about 25 nm thick was formed upon this 8 inch size silicon wafer. Then 368 two-layer gate electrodes of 5 mm diameter were formed upon this oxide layer comprising an upper layer of aluminum and a lower doped layer. Into each of these respective MOS diodes were injected numerous carriers from the substrate silicon as DC polarized voltage was applied between the electrodes at the aluminum layer and the substrate silicon backside. This voltage was ramped upward step-wise in electric field increments equivalent to 0.25 MV/cm each. Holding period for each step was 200 msec as leakage current was measured as the voltage gradually increased. The value of applied voltage when leakage current reached 1 $\mu A/cm^2$ was placed into one of three categories as shown in Table 2: less than 6 MV/cm, between 6 and 8 MV/cm, and greater than 8 MV/cm.

[0034] Moreover, an eight inch size mirror polished silicon wafer was produced from the same silicon single crystal in the same manner. Then 368 dynamic-type RAM were formed upon this wafer using 1.3 μm design rule. Bit failure was measured at a refresh time period (time period between a given injection of charge and the following injection of charge) of 512 cycles per 8 msec. The resultant refresh failure rate is shown in Table 2.

[0035] <Working Example 5> Figure 5 shows a CZ method type pulling apparatus for use for the present invention. Within this figure, a freely rotatable graphite crucible 3 was disposed within a chamber 2 equipped with a gas discharge port 1 and a (non-illustrated) gas feed port. A silica glass crucible 4 was inserted into this crucible 3. The size of graphite crucible 3 and silica glass crucible 4 was 20 inches. A (non-illustrated) pull cable was placed above these crucibles and held a seed crystal by means of a chuck 5 at the tip of the pull cable. Moreover, a heater 6 and carbon fiber molded insulation

member 7 were placed at the perimeter of the crucibles. An inverted cone-shaped radiation shield 13 was placed surrounding crystal 8 from the solid-melt interface upward. Furthermore, in order to restrict cooling rate of the post-solidification silicon single crystal to a certain range, a 260 mm inside diameter and 100 mm tall crystal heater 10 was mounted within the furnace so as to surround silicon single crystal 8. During the entire time period between pulling of the crown region until formation of the tail region, 15 kW was applied to this heater. Also in order to improve heating of silicon crystal 8 by the heater, a thermal insulator 12 was placed surrounding the heater. In order to cause cooling of the crystal immediately above crystal heater 10, the head was squared off rather than given a dome shape. After a 75 kg charge of polysilicon loaded into this silica glass crucible 4 was melted, a 6 inch size silicon single crystal was pulled at a pull rate of 0.8 to 1.0 mm/minute. Cooling rate was controlled in the range indicated by Table 1.

[0036] This silicon single crystal was processed by the normal processing method comprising slicing, edge rounding, lapping, etching, and polishing. Thereafter ammonia-type washing ($NH_4OH : H_2O_2 : H_2O = 3 : 1 : 10$) was carried out. Temperature of the washing solution was 80°C, and a single wash was performed for 20 minutes. Etch pits generated upon this wafer were then measured using a laser-type particle counter (LS600, manufactured by Hitachi Electronics Engineering Corp.). These results are shown in Table 1 and Table 2.

[0037] Moreover, an oxide layer about 25 nm thick was formed upon this 6 inch size silicon wafer. Then 200 two-layer gate electrodes of 5 mm diameter were formed upon this oxide layer comprising an upper layer of aluminum and a lower doped layer. Into each of these respective MOS diodes were injected numerous carriers from the substrate silicon as DC polarized voltage was applied between the electrodes at the aluminum layer and the substrate silicon backside. This voltage was ramped upward step-wise in electric field increments equivalent to 0.25 MV/cm each. Holding period for each step was 200 msec as leakage current was measured as the voltage gradually increased. The value of applied voltage when leakage current reached 1 $\mu A/cm^2$ was placed into one of three categories as shown in Table 2: less than 6 MV/cm, between 6 and 8 MV/cm, and greater than 8 MV/cm.

[0038] Moreover, a six inch size mirror polished silicon wafer was produced from the same silicon single crystal in the same manner. Then 200 dynamic-type RAM were formed upon this wafer using 1.3 μm design rule. Bit failure was measured at a refresh time period (time period between a given injection of charge and the following injection of charge) of 512 cycles per 8 msec. The resultant refresh failure rate is shown in Table 2.

[0039] <Comparative Example 1> Figure 6 shows a CZ method type pulling apparatus for use for this comparative example. Within this figure, a freely rotatable graphite crucible 3 was disposed within a chamber 2 equipped with a gas discharge port 1 and a (non-illustrated) gas feed port. A silica glass crucible 4 was inserted into this crucible 3. The size of graphite crucible 3 and silica glass crucible 4 was 16 inches. A (non-illustrated) pull cable was placed above these crucibles and held a seed crystal by

means of a chuck 5 at the tip of the pull cable. Moreover, a heater 6 and carbon fiber molded insulation member 7 were placed at the perimeter of the crucibles. After a 45 kg charge of polysilicon loaded into this silica glass crucible 4 was melted, a 6 inch size silicon single crystal was pulled at a pull rate of 0.8 to 1.3 mm/minute. Cooling rate was in the range indicated by Table 1.

[0040] This silicon single crystal was processed by the normal processing method comprising slicing, edge rounding, lapping, etching, and polishing. Thereafter 10 minutes of ammonia-type washing ($NH_4OH : H_2O_2 : H_2O = 1 : 1 : 5$) was carried out twice for at total wash time of 20 minutes at a washing solution temperature of 80°C. Etch pits generated upon this wafer were then measured using a laser-type particle counter (LS600, manufactured by Hitachi Electronics Engineering Corp.). These results are shown in Table 1 and Table 2.

[0041] Moreover, an oxide layer about 25 nm thick was formed upon this 6 inch size silicon wafer. Then 200 two-layer gate electrodes of 5 mm diameter were formed upon this oxide layer comprising an upper layer of aluminum and a lower doped layer. Into each of these respective MOS diodes were injected numerous carriers from the substrate silicon as DC polarized voltage was applied between the electrodes at the aluminum layer and the substrate silicon backside. This voltage was ramped upward step-wise in electric field increments equivalent to 0.25 MV/cm each. Holding period for each step was 200 msec as leakage current was measured as the voltage gradually increased. The value of applied voltage when leakage current reached 1 $\mu A/cm^2$ was placed into one of three categories as shown in Table 2: less than 6 MV/cm, between 6 and 8 MV/cm, and greater than 8 MV/cm.

[0042] Moreover, a six inch size mirror polished silicon wafer was produced from the same silicon single crystal in the same manner. Then 200 dynamic-type RAM were formed upon this wafer using 1.3 μm design rule. Bit failure was measured at a refresh time period (time period between a given injection of charge and the following injection of charge) of 512 cycles per 8 msec. The resultant refresh failure rate is shown in Table 2.

[0043] <Comparative Example 2> Figure 7 shows a CZ method type pulling apparatus for use for this comparative example. Within this figure, a freely rotatable graphite crucible 3 was disposed within a chamber 2 equipped with a gas discharge port 1 and a (non-illustrated) gas feed port. A silica glass crucible 4 was inserted into this crucible 3. The size of graphite crucible 3 and silica glass crucible 4 was 22 inches. A (non-illustrated) pull cable was placed above these crucibles and held a seed crystal by means of a chuck 5 at the tip of the pull cable. Moreover, a heater 6 and carbon fiber molded insulation member 7 were placed at the perimeter of the crucibles. An inverted cone-shaped radiation shield 13 was placed surrounding crystal 8 from the solid-melt interface upward. After a 50 kg charge of polysilicon loaded into this silica glass crucible 4 was melted, a 6 inch size silicon single crystal was pulled at a pull rate of 1.3 to 1.7 mm/minute. Cooling rate was controlled in the range indicated by Table 1.

[0044] This silicon single crystal was processed by the normal processing method comprising slicing, edge rounding, lapping, etching, and polishing. Thereafter ammonia-type washing (NH_4OH : H_2O_2 : H_2O = 0.2 : 1 : 10) was carried out. Temperature of the washing solution was 80°C, and 2 washes (10 minutes each) were performed for a total of 20 minutes of washing time. Etch pits generated upon this wafer were then measured using a laser-type particle counter (LS600, manufactured by Hitachi Electronics Engineering Corp.). These results are shown in Table 1 and Table 2.

[0045] Moreover, an oxide layer about 25 nm thick was formed upon this 6 inch size silicon wafer. Then 200 two-layer gate electrodes of 5 mm diameter were formed upon this oxide layer comprising an upper layer of aluminum and a lower doped layer. Into each of these respective MOS diodes were injected numerous carriers from the substrate silicon as DC polarized voltage was applied between the electrodes at the aluminum layer and the substrate silicon backside. This voltage was ramped upward step-wise in electric field increments equivalent to 0.25 MV/cm each. Holding period for each step was 200 msec as leakage current was measured as the voltage gradually increased. The value of applied voltage when leakage current reached 1 $\mu A/cm^2$ was placed into one of three categories as shown in Table 2: less than 6 MV/cm, between 6 and 8 MV/cm, and greater than 8 MV/cm.

[0046] Moreover, a six inch size mirror polished silicon wafer was produced from the same silicon single crystal in the same manner. Then 200 dynamic-type RAM were formed upon this wafer using 1.3 μm design rule. Bit failure was measured at a refresh time period (time period between a given injection of charge and the following injection of charge) of 512 cycles per 8 msec. The resultant refresh failure rate is shown in Table 2.

[0047]
[Table 1]

	Cooling rate during silicon single crystal pulling (°C/minute)			Quartz crucible diameter (inches)	Silicon crystal diameter (inches)	Count of etch pits after mirror polishing and ammonia-type wash (count / wafer)				
	1200°C - 950°C	Minimum cooling rate within 1200°C - 950°C	950°C - 800°C			0.10 - 0.11 μm	0.11 - 0.13 μm	0.13 - 0.16 μm	0.16 - 0.20 μm	> 0.20 μm
Working example 1	2.0 - 1.0	1.0	2.0 - 1.4	16	6	188	257	132	24	8
Working example 2	1.6 - 0.9	0.9	1.5 - 1.2	18	8	280	394	270	55	7
Working example 3	1.4 - 0.8	0.8	1.6 - 1.1	18	6	129	186	212	90	14
Working example 4	1.2 - 0.6	0.6	2.0 - 1.0	22	8	177	199	147	121	75
Working example 5	1.0 - 0.4	0.4	2.6 - 0.5	20	6	28	45	46	44	52
Comparative example 1	3.0 - 1.8	1.8	1.8 - 1.5	16	6	518	387	125	11	1
Comparative example 2	4.0 - 2.8	2.8	2.8 - 2.0	18	6	334	224	25	1	1

[0048]
[Table 2]

	Etch pit ratio (--)		Oxide layer breakdown voltage fraction (%)			Refresh failure rate of MOS type dynamic RAM (%)
	0.13 μm / 0.11 μm	0.13 μm / 0.10 μm	< 6MV/cm	6 - 8 MV/cm	> 8MV/cm	
Working example 1	0.39	0.27	22	48	30	2 - 9
Working example 2	0.46	0.33	20	55	25	1 - 9
Working example 3	0.63	0.50	19	32	49	0 - 8
Working example 4	0.63	0.48	10	36	54	0 - 7
Working example 5	0.76	0.66	5	35	60	0 - 5
Comparative example 1	0.26	0.13	43	44	13	5 - 15
Comparative example 2	0.11	0.05	69	30	1	7 - 20

[0049]
[Results of the Invention] The silicon wafer of the present invention is a silicon wafer that has few harmful defects such as those that cause pn junction leakage failure and oxide layer breakdown voltage failure when devices are formed. In particular, the silicon wafer of the present invention is suitable for production of highly integrated devices with good yield.

[0050] Moreover, the crystal evaluation method of the present invention, by the simple use of a commercial laser-type particle counter, makes possible easy and non-destructive evaluation of electrical characteristics of the silicon wafer without performance of complex heat treatment. Therefore, an improved yield can be anticipated if this method is used for shipping inspection or silicon wafer quality control during the silicon manufacturing step. If the silicon wafers are separated and graded beforehand according to the evaluation method of the present invention just prior to the device manufacturing step, then the silicon wafers can be separated according to the degree of device integration, and overall device yield can be increased.

[0051] In this manner, the present invention is excellent for contributing to production of highly integrated devices with good yield.

[Simple Explanation of Figures]

[Figure 1] This shows schematically construction of a single crystal pulling device used for working example 1 of the present invention.

[Figure 2] This shows schematically construction of a single crystal pulling device used for working example 2 of the present invention.

[Figure 3] This shows schematically construction of a single crystal pulling device used for working example 3 of the present invention.

[Figure 4] This shows schematically construction of a single crystal pulling device used for working example 4 of the present invention.

[Figure 5] This shows schematically construction of a single crystal pulling device used for working example 5 of the present invention.

[Figure 6] This shows schematically construction of a single crystal pulling device used for comparative example 1.

[Figure 7] This shows schematically construction of a single crystal pulling device used for comparative example 2.

[Explanation of Items]

1	....	gas discharge port
2	....	(dome-shaped) water-cooled chamber
3	....	graphite crucible
4	....	silica glass crucible
5	....	seed crystal chuck
6	....	heater
7	....	thermal insulator
8	....	silicon single crystal
9	....	thermal reflector
10	....	crystal heater
11	....	(flat top) water-cooled chamber